IDesignSpec™

AGNISYS
SYSTEM DEVELOPMENT WITH CERTAINTY

Executable Register Design Specification to sign-off quality code

How much time do you spend creating design files, and verification environments that could be saved by automation? How do you bridge the gap between specification and development, verification and firmware?

Complex hardware IP or SoC can have hundreds to thousands of configuration and status registers. An accurate memory map description and its interface to standard buses is needed by design, verification, firmware, diagnostics, tech-pubs, and customers. IDesignSpec enables teams to describe these registers and sequence, in specification ONCE and automatically generate signoff quality standard/custom code and documentation from it, thus improving team productivity and quality of results.

Generated Outputs:

- Design: SystemVerilog, Verilog, VHDL, SystemC
  Register Bus interface: ARM AMBA®, AXI, AHB, APB,
- Avalon®, Wishbone, OCP-IP, I2C*, Token Ring*
- Verification: UVM, OVM, VMM, SV Header, Verification plan, UVM-SystemC
- Software: C/C++ API and header files
- Documentation: HTML, SVG, MS Word®, MS Excel®, PDF, Datasheet
- Standards: IP-XACT, SystemRDL, CMSIS-SVD

Key Features:

- Create outputs right from the register specification
- Self-checking templates prevent errors from entering the flow
- Generate customized documentation and code
- Outputs are totally customizable using Tcl or XSLT
- Handles multi-dimensional registers
- Support for channelization, low-power RTL and special registers, constraints, coverage, back-door access
- Auto generation of the complete verification environment, over and above UVM including bus agents, virtual sequencers, RTL, associated tests, and an annotated verification plan
- Supports ARM AMBA® and other standard buses

Benefits:

- Create synthesizable code for registers and bus interface right from the specification
- Get a jump start for Device Driver, Firmware and application software development
- Automatically verify control & configuration registers in the IP & SoC design
- Automatically create documentation for customers and Tech-Pubs
- Improve productivity of engineers and quality of results
- Create parameterized outputs For greater reuse

Imports:

IP-XACT, System-RDL, RALF, CSV, MS Excel, MS Word, Custom XML, Framemaker, Formatted Text Files

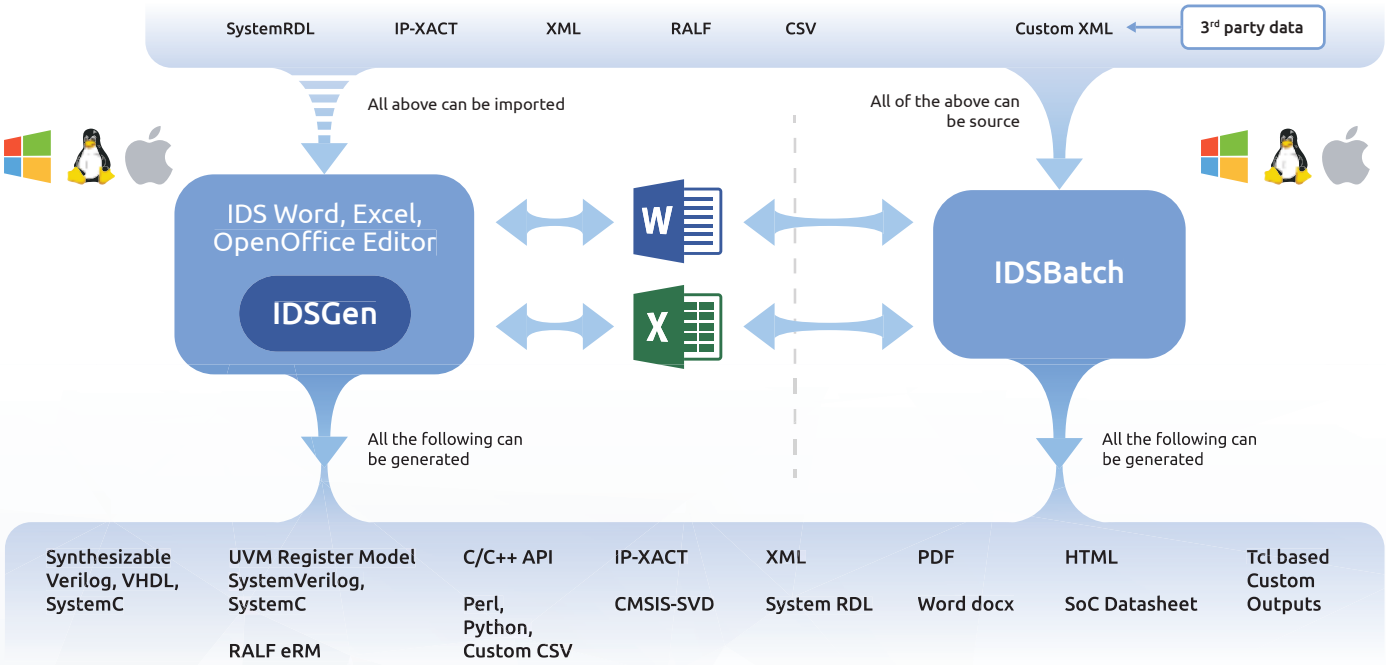
User Interface:

Plugins for MS Word, MS Excel, Libre Office, OpenOffice
Command line mode for Linux, Windows and Mac Platforms

Demo: http://www.agnisys.com/register-verification-demonstration-channel/

IDesignSpec Spec to Sign-off:

IDesignSpec™ is an award winning product that helps IP/SoC Design architects and engineers to create executable specification for registers and automatically generate output for SW/HW teams. The exceptional innovation comes in the simplicity of the solution as the specifications can be written in MS Word, MS Excel, LibreOffice with IDesignSpec editor Plugin or text based industry standard formats like SystemRDL, RALF, IP-XACT. IDesignSpec captures simple as well as special registers, signals, interrupts, and then generates synthesizable RTL code and interfaces to ARM AMBA® buses like AXI, AHB, APB, AHB3Lite and other standard buses.



IDesignSpec Editors - Word & Excel for creating your register specification

Features	Description
Editing Capability	Normal editing capabilities of MS Word and Excel
Check capability in the Document	Checks the spec on-the-fly and annotates the addresses
Customize templates	User customizable templates for registers, register group, blocks, chip and system
References	Ability to add references to other registers & documents
Table of register map insertion	Automatic Register Map insertion
Enum and Defines	Ability to add Enumerations and Define
Property Hints	Ability to see all properties - helps aid spec creation

IDS/Generator – Windows/Linux/Mac for output generation

Features	Descriptions	Professional	Advanced
Register specs imports (in addition to Word, Excel)			
System RDL	Import SystemRDL	Yes	Yes
XML(XRSL)	Our standard XML(XRSL) input	Yes	Yes
Excel/CSV	Excel/Comma separated values files generated by any spreadsheet tool	Yes	Yes
IP-XACT V1.5, V1.4	IP-XACT IEEE 1685.2009 (V1.5) and v1.4	Yes	Yes
RALF	Register Abstraction Layer format by Synopsys	Yes	Yes
Custom XML	Can import any custom XML	-	Yes

RTL Outputs			
Verilog	Synthesizable Verilog model	Yes	Yes
SystemVerilog	Synthesizable SV model	Yes	Yes
VHDL Alternative 1	With records	Yes	Yes
VHDL Alternative 2	With multi-dimensional signals	Yes	Yes
SystemC (RTL)	Synthesizable SystemC model	-	Yes
SystemC (UVM)	UVM-SystemC model	-	Yes
SystemC (VP)	SystemC Virtual Prototype	-	Yes
Verification Outputs			
UVM	UVM Register model	Yes	Yes
OVM	OVM Register model	Yes	Yes
VMM	RAL Model	Yes	Yes
eRM	eRM Register model	Yes	Yes
Verification Plan	IVerifySpec Verification plan	Yes	Yes
Data Structure Outputs			
Perl	Block/Chip level Data Structure in Perl	Yes	Yes
Python	Block/Chip level Data Structure in Python	Yes	Yes
Industry Standard Outputs			
XML(XRSL)	Standard XML(XRSL) output	Yes	Yes
IP-XACT	IP-XACT IEEE 2009, 2014 (V1.5) and v1.4 standard output	Yes	Yes
System-RDL	System RDL1.0 output	Yes	Yes
CMSIS-SVD V1.2	CMSIS- System View Description	-	Yes
Header File Outputs			
SV Header	System Verilog Header	Yes	Yes
C Alternative 1	With union and structures	Yes	Yes
C Alternative 2	With macros	Yes	Yes
MISRA C	MISRA 2004 compliant	-	Yes
Documentation Outputs			
HTML Alternative 1	Without graphics using HTML 4	Yes	Yes
HTML Alternative 2	With graphics using HTML 5	Yes	Yes
SVG	Registers shown graphically	Yes	Yes
PDF	PDF documentation for easy sharing	Yes	Yes
MS Word	Ability to convert any format into MS Word	Yes	Yes
Custom PDF	PDF documentation that can be customized	-	Yes
Advanced Features			
Tcl API	A Tcl language API can generate any custom output or run any custom check	Yes	Yes
Support for different field access types	Software can access registers in a variety of ways (32)	Yes	Yes
Turbo	Generates all the outputs from without annotation hence it is faster	Yes	Yes
Multi-Dimensional Registers	Possible to create non-regular multi-dimensional arrays of register	Yes	Yes
References to support SoC development	Create references to IP level specifications	Yes	Yes
Variants	Create multiple derivative outputs from a single specification	Yes	Yes
Special controls signals	Special user defined control signals	-	Yes
Interrupts	Interrupt logic generator	-	Yes^
Constraint specifications	User specified constraints can be set	-	Yes
Parameterization	Enables run-time customization of generated outputs	-	Yes
Low Power RTL	Low power logic generation.	-	Yes
Multiple Bus Domains	Specify registers on multiple bus domains	-	Yes
Custom circuitry	Ability to connect the registers arbitrarily	-	Yes^

Datasheet Generation	Special features for datasheet generation	-	Yes
Memory Technology Mapping	Ability to instantiate target memory components automatically	-	Yes
Signals	Ability to describe additional ports/bus definition in a Block/Chip	-	Yes
Clock Domain Crossing	Supported circuitry for CDC	-	Yes
Special Registers			
Shadow Register	Data written to a register is copied to another register	-	Yes
RO-WO Register pair	Registers with read-only and write-only access sharing the same address	-	Yes
Shared Register	Same register available in multiple address maps	-	Yes*
Aliased Register	A register accessible at two locations in an address map	-	Yes
Locked Register	Changes to the register-field access based on some input signal or value of another register field.	-	Yes
Trigger Buffer Register	Wide registers with atomic reads and writes triggered by an event	-	Yes
Indirect Register	Several types of indirect registers are possible	-	Yes
Counters	Create up-down counters with saturation and threshold	-	Yes
External Register	User Defined	-	Yes
Paged Register	Paged Block and Register	-	Yes^
FIFO Registers	Create FIFO registers	-	Yes
IDS Batch is supported on Linux, Windows, Mac OS and Solaris. IDS Word and IDS Excel are supported on Windows.			
**Implemented in UVM only, ^Implemented in RTL only*			

Evaluate a Full version of IDesignSpec at: *http://www.agnisys.com/idesignspec-evaluation-form-2/*

Comparative Analysis of IDesignSpec with Other Solutions: *https://www.agnisys.com/comparison-with-idesignspec/*

Automate a Complete Register Verification Environment

ARV™ is an enhancement product to IDesignSpec™ that expands an already powerful register specification solution with capability to automate the register specification-creation-verification process for ARM based SoCs, IP and FPGA semiconductor projects. ARV saves semiconductor teams time and improves quality by enabling complete code coverage for design registers that are the key integration point for semiconductor design, IP, software and interfaces. ARV-Formal uses formal tools to ensure that Register operations conform to the user specification and ARM standards. ARV-Sim can use Questa® VIP to create a UVM based simulation environment to verify the registers automatically.

By Far the Most Comprehensive Register Automation Tool in the World

More details on this can be found in the Agnisys white paper:
http://www.agnisys.com/automate-complete-register-verification-environment/

Agnisys Inc. is a leading Electronic Design Automation (EDA) supplier of innovative software to solve complex design and verification problems for system development with certainty. IDesignSpec™ (Register Generator), ISequenceSpec™ (Portable Sequence Generator), SoC-E™ (SoC Design Intent Verification), DVinsight™ (Smart Editor for SV/UVM) enable design and verification teams to improve productivity and quality.

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