AGNISYS

SYSTEM DEVELOPMENT WITH CERTAINTY

DEVELOPMENT TOOLS FOR IP, SOC AND FPGA TEAMS

Innovative products

–

No learning curve

–

Simple License model

–

Free Customer Enhancements

Agnisys, Inc.

http://agnisys.com
sales@agnisys.com

+1 855-VERIFYY

75 Arlington St. Suite 500
Boston, MA – 02116

IDesignSpec™

Executable Register Design Specification to Sign-off Quality Code

IDesignSpec is the most comprehensive addressable register specification and generation tool in the industry.

- 100+ Outputs out-of-the-box
- 20+ Inputs out-of-the-box
- 100+ Properties & Configurations
- Maximum variety of special registers including indirect, shadow, alias, counters, locked, alternate, wide, paging, shared, virtual, FIFO, external, interrupts
- Maximum variety of inputs and outputs to suite every need
- Windows®, Linux, Mac®
- Command-line or Plug-in
- IP-XACT, SystemRDL, Word®, Excel®, OpenOffice, GoogleDocs, RALF, CSV, …
- Bus support : AMBA AXI, AHB, APB, Avalon, Wishbone, OCP-IP, I2C, SPI

Improve Quality, Save Time & $$

ARV™

Automatic Register & Memory Verification

ARV automatically and comprehensively verifies the registers and memory in a System, saving valuable verification resources.

- Complete verification of Registers and Memory in IP, SoC, FPGA
- Automatic generation of
  - UVM environment (Bus agents, adapter, …)
  - Positive & Negative Sequences
  - Annotated Verification Plan
  - Assertions
  - Complete Verification Report
  - Uses Simulation and Formal tech.
- Code Coverage and Functional Coverage reaches close to 100% out of the box automatically
- Special registers are verified too
- Register definitions in IP-XACT, SystemRDL, RALF and other IDesignSpec formats.

Improve Quality, Save Time & $$

DVinsight™

Smart Editor for SV/UVM & SystemRDL

DVinsight is a smart editor for faster, bug-free development of UVM based SV code base and for SystemRDL based register specification.

- Built-in UVM checks
- On-the-fly linting checks
- Uses inline editors to maintain context
- VIM, Emacs modes support finger memory
- Link to popular simulators Cadence®, Mentor®, Synopsys®
- Availability : Linux (RedHat 7, Ubuntu 10), Windows®

Improve Quality, Save Time & $$

AGNISYS

SYSTEM DEVELOPMENT WITH CERTAINTY

DEVELOPMENT TOOLS & SERVICES FOR IP, SOC AND FPGA TEAMS

Thought leadership

–

Simple Pricing model

–

Easy company to work with

–

Global support network

–

Extensive customer base

Agnisys, Inc.

http://agnisys.com
sales@agnisys.com

+1 855-VERIFYY

75 Arlington St. Suite 500
Boston, MA – 02116

ISequenceSpec™

Portable Sequence Generator for UVM, Firmware & Validation

ISequenceSpec is a unique tool in the industry with which user can create portable sequences. These sequences will work in Verification (UVM), Firmware, Validation and ATE.

- A single source specification of sequence format ensures synchronization between all stages of development.
- Quickly run the verification test sequences in the lab and lab sequences in verification env.
- Reproduce the post-silicon failure test cases in the simulation environment for faster debug.
- Use register definitions in IP-XACT, SystemRDL, RALF and other IDesignSpec formats.
- Avalon, Wishbone, OCP-IP, I2C, SPI

Improve Quality, Save Time & $$

SoC Enterprise™

SoC Integrator & Database Mgmt.

SoC Enterprise provides a multi-user, multi-platform eclipse and IP-XACT based framework for integrating and building SoCs

- Promotes reuse and collaboration
- Generates
  - Netlist in Verilog, VHDL
  - Formal Assertions for connectivity checks
  - SystemC and UVM verification Environments
  - Datasheet in Word, HTML, PDF
  - Complete UVM based self checking Verification environment for Digital – Analog designs
- Uses word-class graphics package for visualization
- Maintains I/O ports, interconnects, Registers, Sequences, Physical, Electrical parameters, Analog data
- Tcl API available for interface
- Inbuilt DRC checks improve design quality

Improve Quality, Save Time & $$

Consulting/Training

Word Class Services

Agnisys has been providing Consulting and Training services for over a decade.

Consulting Services

- Turn-key Verification environment development
- Coverage model creation
- Coverage closure
- SV-UVM, SystemC, e based verification
- SystemC TLM2 based model development

Training Courses

- System Verilog for Verification (4 days)
- Introduction to UVM (3 days)
- Advanced UVM (2 days)
- System Verilog Assertions (1 day)
- SystemC Modeling with TLM 2.0 (2 days)

Availability

- Throughout the world
- In person or Online

Improve Productivity, Save Time & $$

Version: IDS/2017/2/9