Automatic RegMap Verification (ARV)

AGNISYS
SYSTEM DEVELOPMENT WITH CERTAINTY

UVM/Formal based Addressable Register & Memory Map Verification

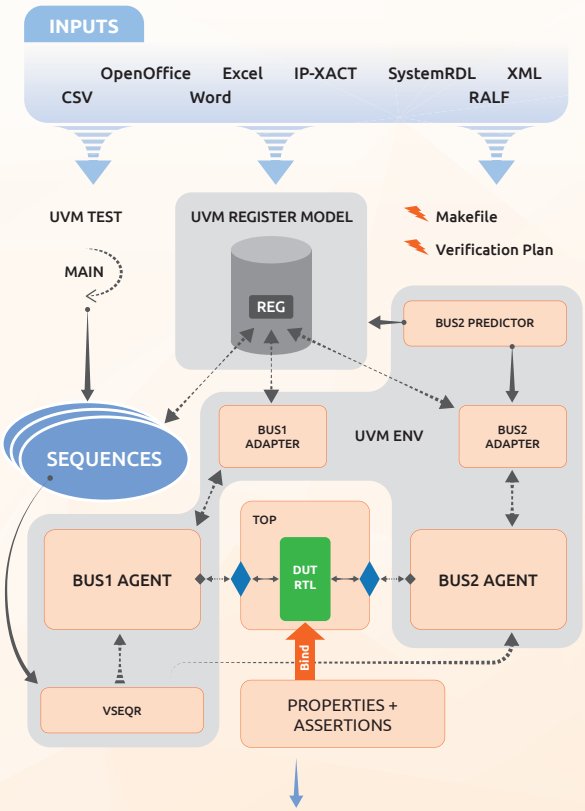
NO MORE Manual Verification

Register and Memory map Verification is a time and resource intensive activity that can be fully automated.

Out-of-the-box standard UVM sequences give about 60% coverage for register maps. To get to 100% functional and code coverage requires verification teams to spend close to 50% of their verification effort. This time can be saved by ARV.

ARV automatically generates:

- Complete UVM based verification environment
  components, hdl_paths, covergroups, constraints, illegal bins, …
- Sequences for positive and negative functionality
- Verification Plan, Makefiles for all simulators
- Assertions for register access with a variety of busses
  ARM® AMBA AHB, APB, AXI, Avalon®, OCP-IP, Wishbone, …
- Register-centric verification report



~ 100% Coverage Out-of-Box

Even though verification teams use automated UVM register model generation, they need ARV for absolute proof of correct integration and working of the Register Map.

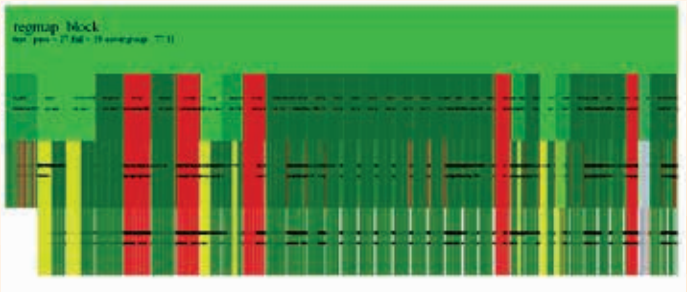
ARV can take the following type of input: SystemRDL, IP-XACT, Word, Excel, OpenOffice, RALF, CSV, Custom-XML, …

Benefits:

- ~100% Register and Memory Map Verification saves time
- MemoryMap centric verification report gives focused and accurate status
- Automatic verification of all UVM access types & special registers : Indirect, Shadow, Lock, Alias, …
- Provides absolute proof of correct RegMap behavior

Hierarchical RegMap Verification Report

- Interactive, deep-dive, to help quick debug
- Intuitive, natural interface, no learning curve
- Tells you when you can get off the Verification "merry-go-round"



Agnisys Inc. is a leading Electronic Design Automation (EDA) supplier of innovative software to solve complex design and verification problems for system development with certainty. IDesignSpec™ (Register Generator), ISequenceSpec™ (Portable Sequence Generator), SoC-E™ (SoC Design Intent Verification), DVinsight™ (Smart Editor for SV/UVM) enable design and verification teams to improve productivity and quality.

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