

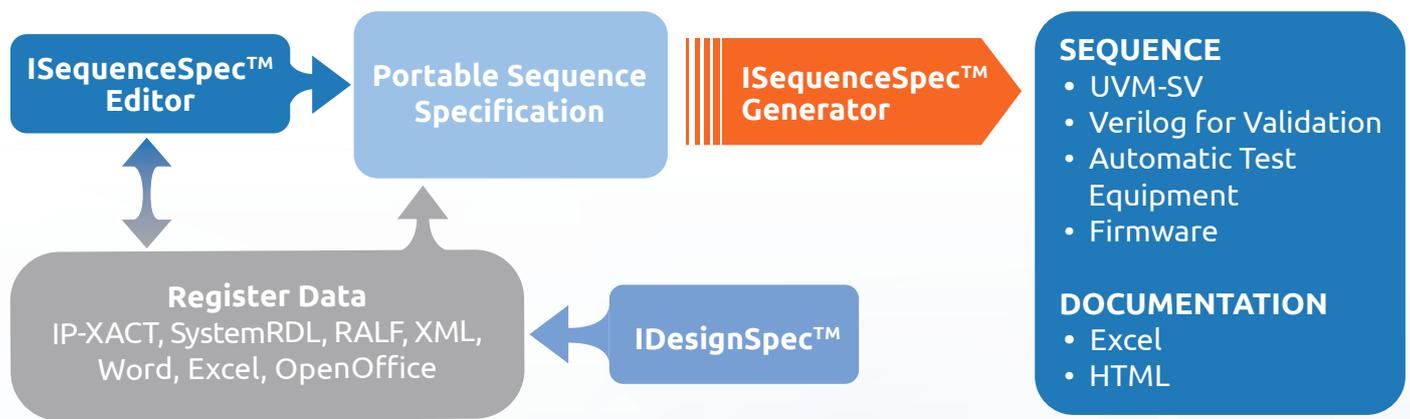
ISequenceSpec™

Portable Sequence Generator for Verification, Firmware & Validation



How much time does your team spend in writing sequences in different languages for the same functionality? How do you bridge the gap between specification and silicon validation?

ISequenceSpec™ enables users to describe the programming and test sequences of a device and automatically generate sequences ready to use from an early design and verification stage to post silicon validation. Sequences are a “set of steps” that involve writing/reading specific bit fields of the registers in the IP/SoC. These sequences can be simple, or complex involving conditional expressions, array of registers, loops, etc. ISequenceSpec helps the user write a single sequence specification and generate the UVM sequences for verification, Verilog sequences for validation, C code for firmware & Device drive development and various output formats for Automatic Test Equipment.



Benefits

- ▶ A single specification format ensures synchronization between various stages of development
- ▶ Quickly run the verification and firmware tests in the lab
- ▶ Quickly run the post silicon failure test cases in the simulation environment
- ▶ Save time by automatically generating the test sequences
- ▶ Keeps each design team member aligned with the updated sequences as the project progresses
- ▶ Interface with popular high level graph based testing automation tools

Features

- ▶ Simple, natural, portable sequence format for multiple IP/cores.
- ▶ Capture sequences at a higher level in-sync with register specification
- ▶ Use register descriptions in standard formats like IP-XACT, SystemRDL, RALF or leverage on IDesignSpec™ integrated flow to use register data
- ▶ Sequence constructs include loops, if-else, wait, arguments, constant, in-line functions
- ▶ Compile, flatten, unroll the sequences
- ▶ Simple to use, no training required

For more details please visit:

<https://www.agnisys.com/products/isequencespec-portable-sequence-generator>

Agnisys Inc. is a leading Electronic Design Automation (EDA) supplier of innovative software to solve complex design and verification problems for system development with certainty. IDesignSpec™ (Register Generator), ISequenceSpec™ (Portable Sequence Generator), SoC-E™ (SoC Design Intent Verification), DVinsight™ (Smart Editor for SV/UVM) enable design and verification teams to improve productivity and quality.

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