

Agnisys IDS-AI™ is your team from specification to first-pass sign-off silicon dramatically faster.

IDS-AI™ is the industry's first agentic AI framework built specifically to understand semiconductor design functional specification, CSR, SoC hierarchy & connectivity and RTL. Instead of stitching together point tools and manual handoffs, you get Agentic AI that drives the entire flow – from golden specification creation to RTL sign-off – on your behalf. It is built on Agnisys' IDesignSpec Suite, which has been refined over the past two decades of production use, so you get the reasoning and productivity of AI with the certainty and accuracy of rule based tools.



THE CHALLENGE & THE SOLUTION

Challenge

Incorrect or incomplete specifications cause ~45% of functional bugs, and spec changes cause another ~30% – leaving only 14% of ASIC projects with first-silicon success.*

Solution

IDS-AI™ combines Agentic AI with Agnisys' proven correct-by-construction automation to create, validate, and continuously refine golden specifications while automating the path from specification to sign-off.

* 2024 Wilson Research Group Study by Siemens EDA

GOLDEN SPECIFICATION TO SIGNOFF

Input

Golden input specification containing SoC/IP and CSR definitions (.md, Word, PDF, HTML, Text, SystemRDL, purpose-built GUI and others).

Output

Auto-generated Implementation-ready RTL, SoC/IP integration and assembly, UVM verification testbenches and tests, validation environments and tests, documentation – all synchronized to the golden specification.

FEATURES & BENEFITS

Feature

- One agentic AI layer across the whole platform
- Natural Language Engineering
- Self-Correcting loop and CSR check for completeness, correctness, and integrity
- Deterministic output generation
- Guaranteed Artifact Synchronization- Keep RTL, verification, firmware, and documentation automatically synchronized from one specification.
- 100% CSR verification coverage
- Flexible deployment (on-premises or remote)

Benefit

- One assistant for spec, design, verification & integration – no tool-hopping
- Describe design intent using prompts instead of manual engineering tasks.
- Improve specification quality and catch defects before coding begins
- Accelerate verified outputs generation and reduce manual engineering effort
- Single source of truth – fewer re-spins, higher predictability
- Achieve sign-off with confidence
- Fits existing flows without forcing a platform switch

Built For

- AI Accelerators
- Automotive SoCs
- Data Center Processors
- Networking Chips
- Storage Controllers
- FPGA Platforms
- Embedded Systems
- Custom ASIC Development

